REMARKS/ARGUMENTS

The applicant thanks the Examiner for entering the amendments to the claims and for the Examiner's comments. The applicant respectfully traverses the obviousness rejection.

Amendment to Claim 12

Claim 12 has been amended to further clarify that the first and second semiconductor dice are directly mounted on and electrically connected to the first and second surfaces of the conductive die pad, respectively. Thus, there are no intervening insulating layers and wiring layers as shown in Hirasawa et al. The amendment is fully supported by the specification and drawings. For example, paragraph [0006] discloses two semiconductor dice connected to the opposite lead frame surfaces by a suitable die attach material such as a silver loaded epoxy adhesive. Thus, examples in the specification show that the conductive silver loaded epoxy directly mounts the semiconductor dice on opposite surfaces of the die pad, as shown in the drawings.

Rejection under 35 U.S.C. §103(a)

With respect to claims 12, 15 and 19, which were rejected as being unpatentable over Hirasawa in view of Rostoker, the cited references fail to establish *prima facie* obviousness either alone or in combination, and Rostoker teaches away from the invention of Hirasawa et al.

In order to establish *prima facie* obviousness, a reference or a combination of references must teach or suggest each and every limitation of a claimed invention. Claim 12, as amended, reads " . . . a first semiconductor die having a first major electrode . . . said first major electrode of said first semiconductor die being directly mounted on and electrically connected to said first major surface of [a] conductive die pad; [and] a second semiconductor die having a first major electrode . . . said first major electrode of said second semiconductor die being directly mounted on and electrically connected to said second major surface of said conductive die pad . . . ."

Hirasawa et al.

Hirasawa et al. fails to teach or suggest that any electrode is "directly mounted on and electrically connected to" any surface of a conductive die pad. Instead, Figs. 2A and 2B show

that one electrode of a semiconductor die 206 is mounted to a layer above the surface of a conductive die pad 201a, which is separated from the die 206 by interposed insulating layers 202, 204. Indeed, Hirasawa et al. teaches that the electrode opposite of the mounting surface of the semiconductor die of Figs. 2A and 2B is electrically connected to the die pad by wire bonds and electrical traces. Indeed, the first major surface of the semiconductor die 206 is mounted on an insulating layer 204, which intentionally prevents any direct connection between the lower surface of the die 206 and the die pad 201a. Thus, Hirasawa et al. fails to teach or suggest every limitation of claim 12.

Now, referring to Figs. 4A-4C, Hirasawa et al. teaches a flip chip 406 connected to second wiring layers 405 through solder bumps 409a. A fixed potential of the flip chip 406 is electrically connected to the die pad 401a by a solder bump 409a, through extending connection 411 formed by through-holes " . . . extending through the lower insulating layer 402 and interlevel insulating layer 404." See column 6, lines 30-34 and lines 43-48. Thus, the lower surface of the flip chip is not directly mounted on the first major surface of the die pad. Instead, Hirasawa et al. teaches that the flip chip is mounted on wiring layers 405, which are necessarily separated from the conductive die pad by insulating layers 402, 404, such that only the fixed potentials, such as the ground potential, are electrically connected to the die pad 401a. Therefore, Hirasawa et al. fails to teach or suggest every limitation of claim 12. Indeed, Hirasawa et al. teaches away from directly mounting the semiconductor die on the surface of said conductive die pad. Specifically, Hirasawa et al. teaches that the semiconductor chips 206, 406 must be separated from the die pad 401a by several layers, including insulating layers 402, 404 and wiring layers 403, 405. This is necessary for the functioning of the die pad 401a as a ground plate. Thus, Hirasawa et al. fails to establish *prima facie* obviousness of claim 12.

In the alternative, if the entire substrate structure of the die pad 401a, the insulating layers 402, 404 and the wiring layers 403, 405 are considered to be a "die pad," which is contrary to the general understanding of the definition of a die pad in the field, then Hirasawa et al. teaches away from a conductive die pad "consisting of a conductive material" as claimed in claim 12, because insulating layers 202, 204, 402, 404 are by necessity non-conductive insulators. Therefore, Hirasawa et al. teaches away from this limitation of claim 12. Regardless, Hirasawa et al. fails to

establish *prima facie* obviousness of claims 12, 15 and 19 and teaches away from the claimed inventions.

Rostoker

Rostoker fails to establish *prima facie* obviousness and teaches away from Hirasawa et al. In Figs. 1A and 1B, Rostoker shows a planar substrate 110 that is nonconductive (column 5, line 50 and column 6, lines 27-29). The conductive traces 112a, 112b, as shown in Fig. 1B, would not be considered by a person of ordinary skill in the field to be a die pad. Instead, the "die pad" 110, 111, as shown in Fig. 1A and Fig. 1C, is taught by Rostoker to be a nonconductive material such as ceramic, FR4 fiberglass, or BT resin, (column 6, lines 27-29). These common substrate materials are insulators. The use of insulating substrates is essential to the invention of Rostoker, which uses conductive wire traces 112a on the surface of the insulating planar substrate 110, 111 to form connections to "very large numbers of connections to relatively small semiconductor dies, such as numbers of connection greater than 500, 600, 700, 800, 900 or 1000." See column 3, lines 18-20. Thus, Rostoker fails to teach "a conductive die pad consisting of a conductive material" and a "first major electrode of said first semiconductor die being directly mounted on and electrically connected to said first major surface of said conductive die pad," as claimed in claim 12. In addition, Rostoker fails to teach or suggest a "first major electrode of said second semiconductor die being mounted and electrically connected to said second major surface of said conductive die pad," as claimed in claim 12. Thus, Rostoker fails to teach or suggest the limitations of claim 12 that are omitted by Hirasawa et al., and neither of the cited references teach or suggest every limitation of the claimed invention alone or in combination. Therefore, Hirasawa et al. and Rostoker, fail to establish *prima facie* obviousness of claim 12.

Teaches Away from Combination

In addition, Rostoker teaches away from the combination of Rostoker and Hirasawa et al. Specifically, Hirasawa et al. requires a conductive die pad, and the teachings of Rostoker teach away from the use of a conductive die pad. Therefore, one of ordinary skill in the art would not combine the teachings of Hirasawa et al. and Rostoker. Thus, claim 12 is also nonobvious over Hirasawa et al. and Rostoker for this reason.

Claims 15 and 19

Claims 15 and 19 depend from claim 12, incorporating all of the limitations of claim 12 and additional limitations. Therefore, for the foregoing reasons, claims 15 and 19 are nonobviousness over Hirasawa et al. and Rostoker.

Claim 19

In addition, claim 19 claims a "first plurality of leads . . . spaced from said conductive die pad" and a "second plurality of leads . . . spaced from said conductive die pad." Rostoker teaches away from "lead frame-type packages," because "it is extremely difficult or impossible to provide a conductive lead frame with any kind of structural integrity when the leads become too small," (col. 2, ll. 60-64). The leads 112a, 112b of Rostoker cannot be "spaced from said conductive die pad" as recited in claim 19, as the leads 112a, 112b of Rostoker rely on support from the substrate 112a, 112b for structural integrity. Thus, for these additional reasons, claim 19 is nonobvious over Rostoker and there is no motivation to combine Rostoker and Hirasawa et al. to achieve the invention in claim 19.

Claims 12, 13 and 16

With regard to claims 12, 13 and 16 as being unpatentable over Hirasawa et al. and Rostoker as applied to claim 12 above, and further in view of Munoz et al., Munoz et al. fails to teach or suggest each of the limitations of claim 12 that are missing from Hirasawa et al. and Rostoker, as previously discussed. Thus, the combination of Hirasawa et al., Rostoker and Munoz et al. fails to establish *prima facie* obviousness of claim 12.

Munoz et al. fails to teach or suggest ". . . a second semiconductor die having a first major electrode . . . of said second semiconductor die being directly mounted on and electrically connected to said second major surface of said conductive die pad;" therefore, Munoz et al. fails to establish *prima facie* obviousness of claim 12, which recites this limitation. Neither Hirasawa et al. nor Rostoker teach or suggest this limitation. Thus, a combination of the cited references fails to establish *prima facie* obviousness.

In addition, Hirasawa et al. teaches away from directly mounting a semiconductor die 206, 406 to a conductive die pad; therefore, there is no motivation to combine Hirasawa et al. and

Munoz et al. to achieve the invention of claim 12. As previously discussed, the invention of Hirasawa et al. teaches interposed insulating and wiring layers between semiconductor devices and the die pad.

In addition, Rostoker teaches away from Munoz et al. because Rostoker teaches that a lead frame such as disclosed in Munoz et al. makes it ". . . it is extremely difficult or impossible to provide a conductive lead frame with any kind of structural integrity . . . ," when making connections as disclosed in Rostoker. See column 2, lines 60-69. Thus, there is no motivation to combine the teachings of Munoz et al. and Rostoker.

Claims 13, 14 and 16

As claims 13, 14 and 16 depend from claim 12, incorporating all of the limitations of claim 12 and additional limitations, Hirasawa et al., Rostoker and Munoz et al. fail to establish *prima facie* obviousness over claims 13, 14 and 16.

Claims 17 and 18

With regard to the rejection of claims 17 and 18, as being unpatentable over Hirasawa et al., Rostoker and Munoz et al. as applied to claim 14 above, and further in view of Adishian, Adishian fails to teach or suggest those limitations omitted by Hirasawa et al., Rostoker and Munoz et al.; therefore, the cited references fail to establish *prima facie* obviousness of claims 17 and 18. Specifically, Adishian fails to teach or suggest electrodes of first and second semiconductor dice being "directly mounted on and electrically connected to" a die pad ". . . such that said first electrode of said first semiconductor die is electrically connected by said conductive material of said conductive die pad to said first electrode of said second semiconductor die and to one of said second plurality of leads or one of said first plurality of leads." Thus, the combined teachings of all of the applied references fail to teach or suggest to one of ordinary skill in the art each and every limitation of claim 12, the independent claim, and the additional limitations of the dependent claims. As claims 17 and 18 depend from claim 12, incorporating all of the limitations of claim 12 and additional limitations, the applied references fail to establish *prima facie* obviousness of claims 17 and 18.

On page 8, the Examiner mentions Golwalker et al.; however, Golwalker et al. is not introduced as a cited reference. In addition, as discussed in the previous amendment and response dated December 19, 2003, the integrated circuits of Golwalker et al. are not electrically connected to the die pad. Instead, Golwalker teaches use of an insulating adhesive bond between the bottom electrodeless surface of integrated circuits and the die pad. The integrated circuits are conventionally bonded, using wire bonds or otherwise, to connect electrodes located under free, top surfaces of the integrated circuits. Thus, Golwalker et al. fails to teach or suggest any of the limitations of claim 12 that are missing from Hirasawa et al., Rostoker and Munoz et al.

For the foregoing reasons, all of the pending claims are nonobvious over the cited references and are now in condition for allowance.

The Applicant respectfully requests that the Examiner enter the amendments to claim 12. The application is now in condition for allowance.

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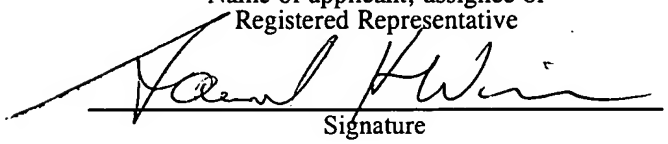

Signature

June 3, 2004
Date of Signature

Respectfully submitted,

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